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FILING DATE: *April 01, 2004*

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13281 U.S.PTO

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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

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☐ Additional inventors are being named on the ^ separately numbered sheets attached hereto

TITLE OF THE INVENTION (280 characters max)

CONSTANT ERASE CURRENT

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ENCLOSED APPLICATION PARTS *(check all that apply)*

☒ Specification *Number of Pages* 8 ☐ CD(s), Number

☒ Drawing(s) *Number of Sheets* 1

☐ Application Data Sheet. See 37 CFR 1.76 ☒ Other (specify) postcard

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT *(check one)*

☐ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check or money order is enclosed to cover the filing fees

☒ The Commissioner is hereby authorized to charge filing fees or credit any overpayment to Deposit Account Number: 05-0649

☐ Payment by credit card. Form PTO-2038 is attached.

FILING FEE AMOUNT ($) 160.00

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☒ No.

☐ Yes, the name of the U.S. Government agency and the Government contract number are:

Respectfully submitted,

Date 01 / Apr / 2004

SIGNATURE

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REGISTRATION NO. *(if appropriate)* 52,388

Docket Number: P-6715-USP

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

SAIFUN

Constant Erase Current Patent

Inventors: Assaf Shappir

Ilan Bloom

Boaz Eitan

11 March 2004

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Constant Erase Current Patent

- The problem
  - The current invoked during NROM cell erasure with constant voltages is characterized by a high peak which quickly subsides. This peak limits the amount of cell which can be erased simultaneously, due to current consumption limits imposed on the memory product.
  - Furthermore, the efficiency of the constant voltage erase pulse also subsides with time. Hence, during the second half of the pulse a current flows from the cell, yet erasure is very weak.
  - The final outcome is a large current consumption during cell erasure, together with an inherent inefficiency of the constant voltage erase pulse.
  - These two drawbacks translate into a reduced erase rate in the NROM memory product both the number of cells which can be erased simultaneously is limited and the duration of the erase pulse must be long enough to compensate for its inefficiency.

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Constant Erase Current Patent

- Solutions to the problem have included:
  - Erasure of smaller cell populations hence the total peak current does not pass the product spec. limitation. The downside of this method is a slower erase rate, as many sub groups must be erased separately, instead of simultaneous erasure of the entire population.
  - Erasure with lower voltages the applied voltages determine the erase current, hence by the reduction the current subsides. The resultant penalty is the reduction of the erase speed (lower voltages → longer erase pulses).
  - Hole injection into the NROM ONO stack mainly above the n^+ junctions to quickly reduce the erase current the erase current is generated at the n^+ junctions of the NROM cell. Reducing the amount of trapped electrons above this region, by hole injection, reduces this current. The downside is that a two step algorithm must be performed: current reduction, followed by efficient erasure (reduction of cell threshold voltage). One way of achieving this is by two sided NROM cell erasure followed by a single sided NROM cell erasure. The final outcome is a slower erase speed, due to the necessity of two stages.

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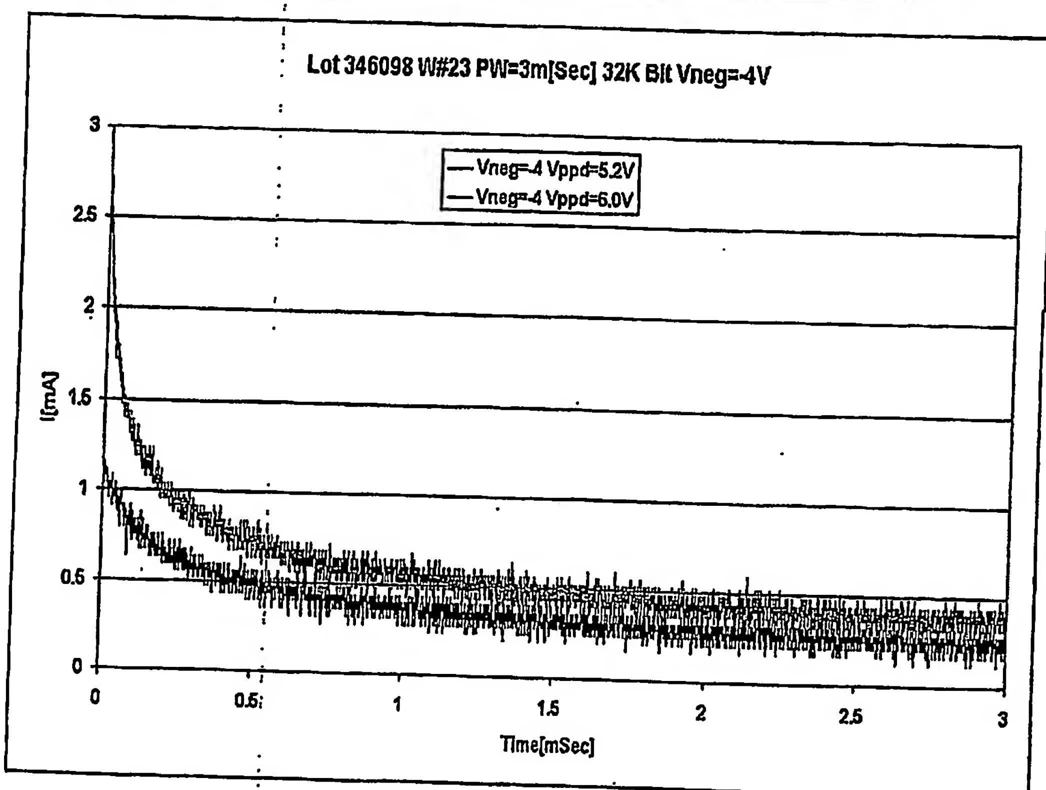
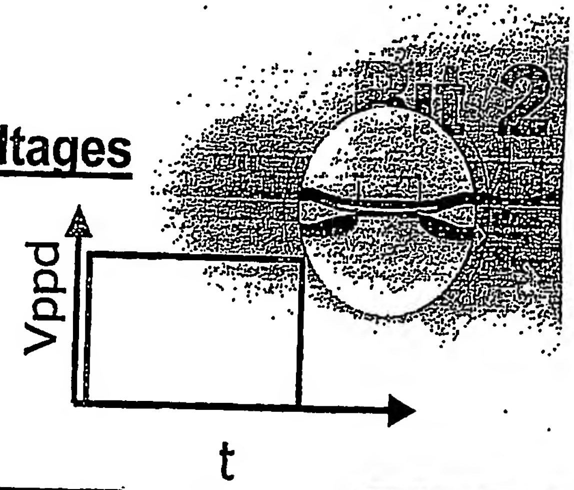
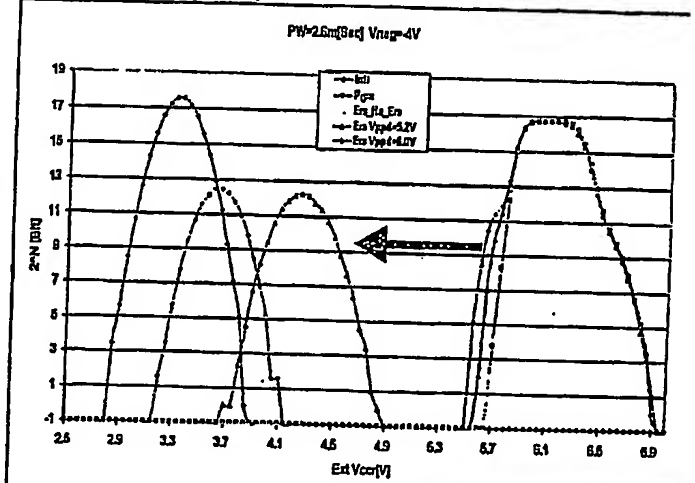
Typical Result square pulse with constant voltages

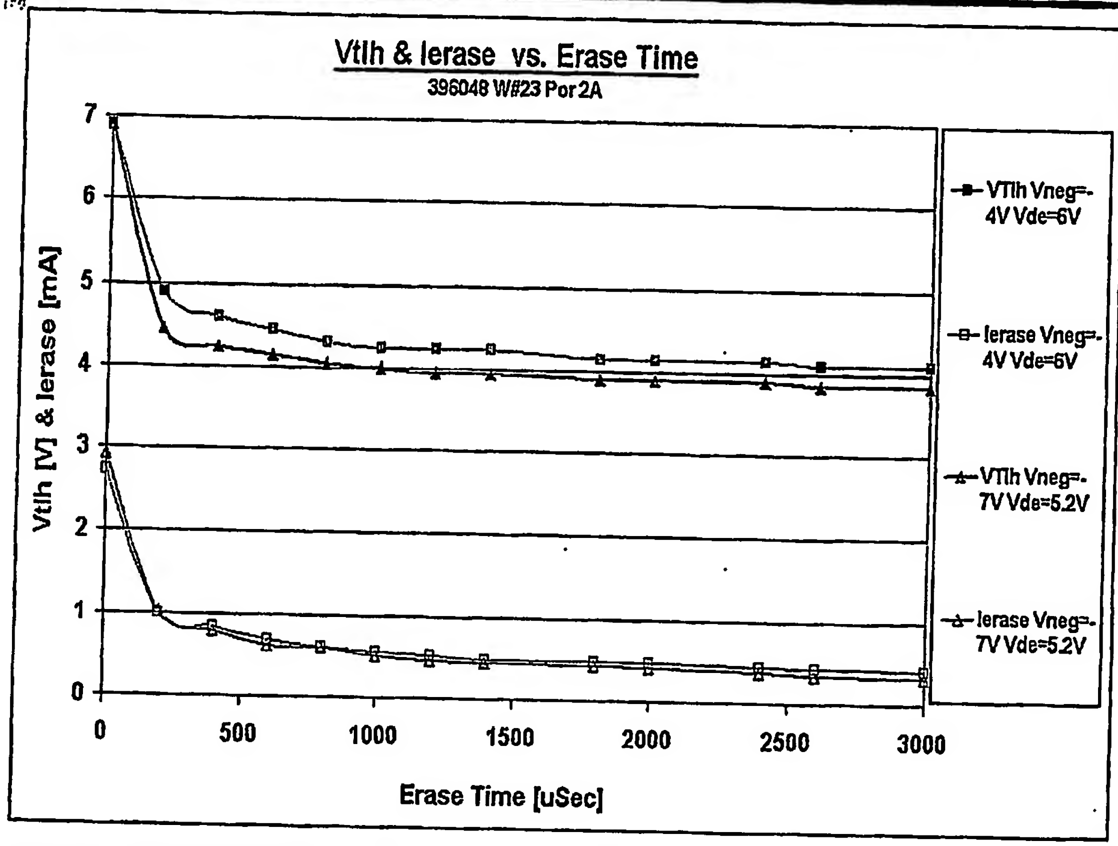






- Two current measurement during 3ms long erase pulses are shown (left) together with the resultant shift of the erased population (32K bits - right).
- The higher the erase pulse voltages (6V vs. 5.2V in the figures) the higher the erase current and the larger the threshold voltage shift (erasure).
- In both case the erase current subsides by ~8× during the pulse.

Erase current vs. Threshold voltage shift



- The above graph shows the reduction of the erase current together with the reduction of the highest threshold voltage in the array population as a function of time during the 3ms erase pulse.
- It can be seen the both the current and the rate of threshold voltage downward shift subside. I.e., erasure becomes inefficient during the course of the erase pulse   current continues flowing (~0.4mA in this example), yet the threshold voltage downward shift is very slow.

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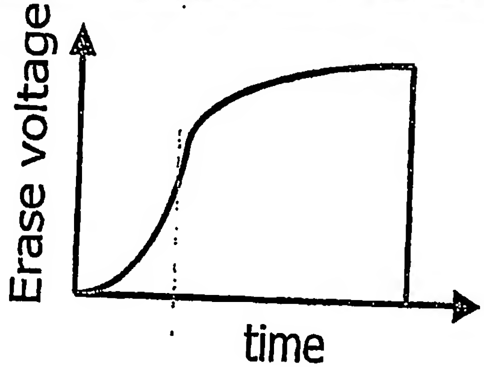
Constant Erase Current - Description



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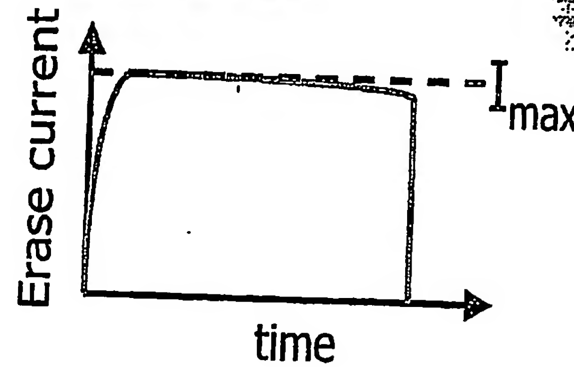
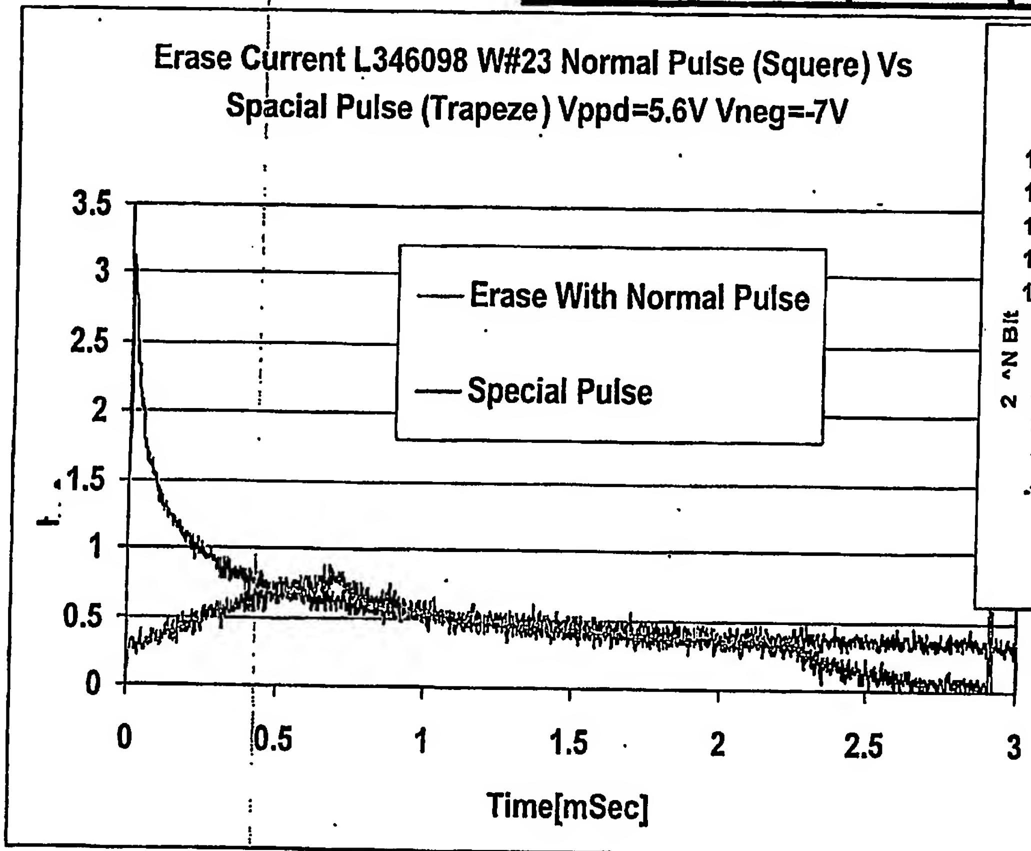
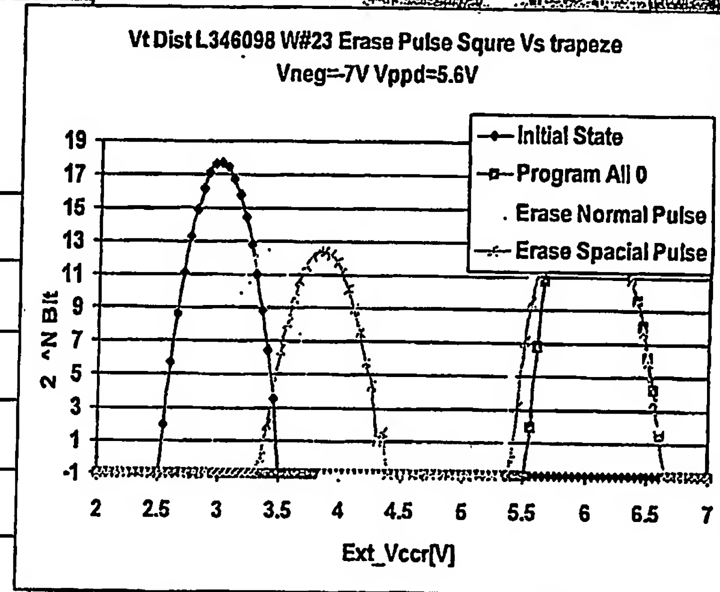


- Applied erase voltages, will be ramped from a low value to the desired voltage level the ramping can be limited to a subgroup of the erase voltages, for example: the array gates are fully biased to the desired level/s, the array well is grounded, the array source lines are floated after grounding and the array drain lines are ramped to the desired level.
- The array current consumption will be continuously monitored and the voltage ramp rate adjusted, by a feedback loop, in order to prevent the current from exceeding a pre-specified limit. Efficient current consumption will be achieved regardless of the data content and the bit count.
- Alternatively, the ramp rate can be set to a predefined level without monitoring the array current consumption the strong peak in the erase current can be thus prevented, but the current level will not be constant (see next slide).
- Ramp may be analog (continuous) or digital (stepping).

Erase voltage ramping example

Square vs. Trapezoid pulse





- In this example the erase current and the induced threshold voltage reduction of two pulse shapes is compared: square drain pulse vs. trapezoid drain pulse (all other terminals were set to fixed voltages).
- It can be seen that while erasure is comparable (right figure) the erase current peak was reduced by ~5×. The erase current is not constant in this case, due to the lack of a current monitoring based voltage feedback loop.

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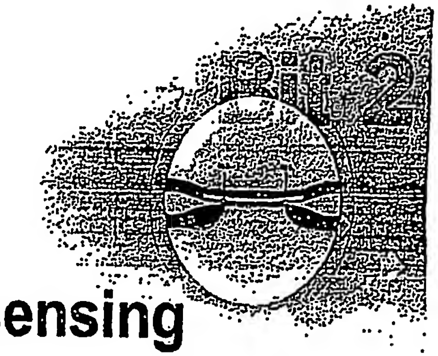
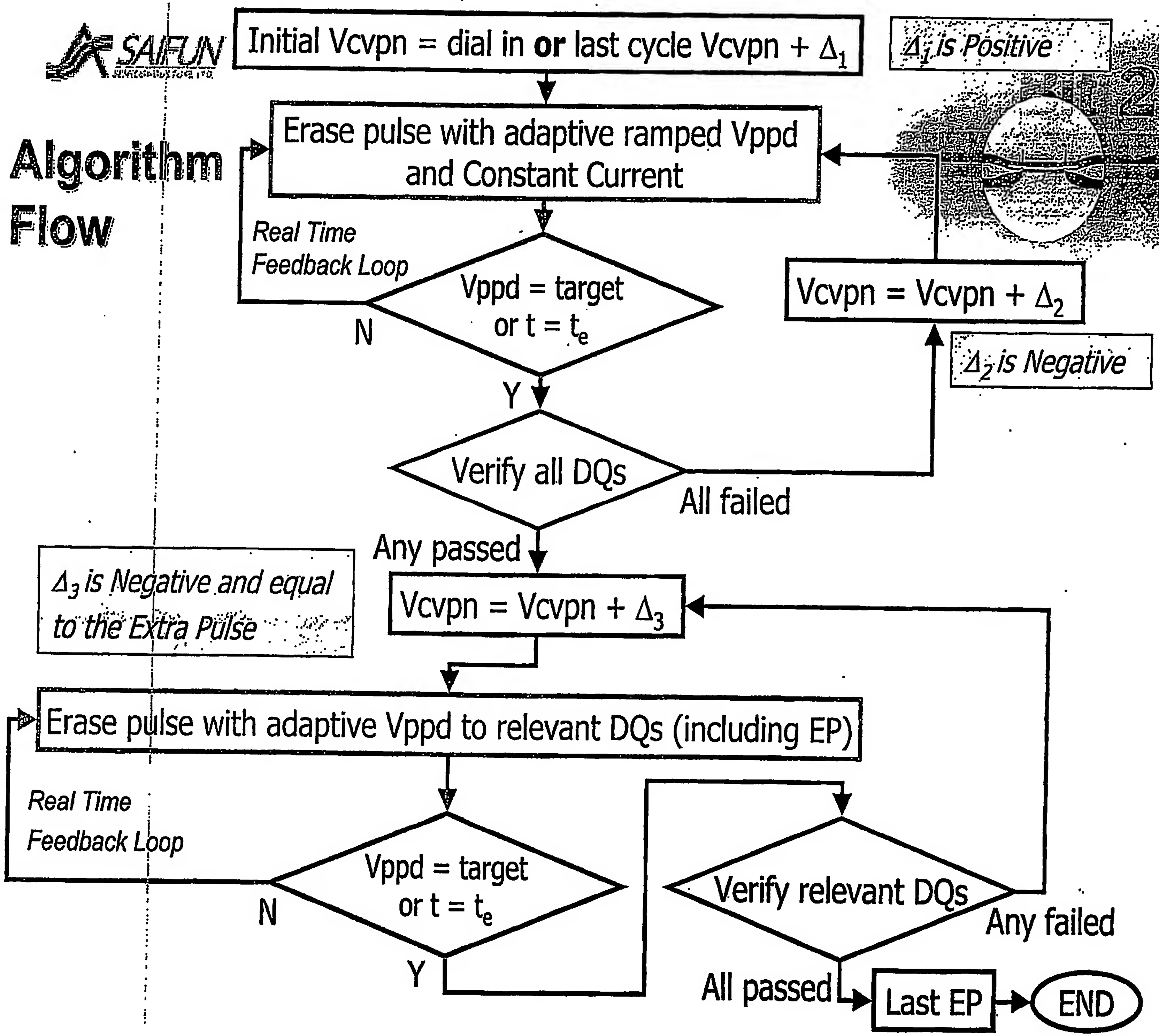


Example

Gate stepping erase algorithm with current sensing

- The array gates will be set to the desired negative level and the drain voltage ramped (alternatively the array gates may be ramped, both drain and gate, etc.).
- The erase pulse is completed when either the designated period is reached (t_e) **or** the designated drain voltage is reached and maintained a short period of time (X μs). Hence the actual pulse duration will be $\leq t_e$.
- Following the erase verify operation, the gate voltage will be incremented.
- An extra pulse is applied after the erase verify level is reached.

Algorithm Flow



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